REMARKS

Claims 1-51 are pending in the present application. Claims 32-51 have been previously withdrawn from consideration. Reconsideration is respectfully requested.

In the outstanding Office Action, claims 1-10 and 15-31 were rejected under 35 U.S.C. Section 102(b) as anticipated by U.S. Patent No. 5,675,170 (Kim et al.); and claims 1, 7 and 11-14 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,642,667 (Magee).

35 U.S.C. Section 102 Rejections

Claims 1-10 and 15-31 were rejected under 35 U.S.C. Section 102(b) as anticipated by Kim et al. Applicant respectfully traverses the rejection.

The Final Rejection includes rejections based on anticipation. "Anticipation under 35 USC §102(e) requires that 'each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.'" *In re Robertson*, 49 USPQ 1949, 1950 (Fed.Cir. 1999).

> "[A]ll words in the claim must be considered in judging the patentability of the claim against the prior art." *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970). As set forth in section 2111 of the MPEP, "claims are interpreted in the broadest reasonable fashion *consistent with the specification.*" (Emphasis added). The Patent and Trademark Office *is required* to take into account whatever enlightenment is afforded by the specification, *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ 2d 1023, 1027-28 (Fed. Cir. 1997). (Emphasis added).

In addition, Applicants note that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[1] *There must be no difference between the claimed invention and reference disclosure* for an anticipation rejection under 35 U.S.C. §102[2] (emphasis added). To properly anticipate a claim, the reference must teach every element of the claim.[3] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[4] "The identical invention must be shown in as complete detail as is contained in the ...claim."[5] In determining anticipation, no claim limitation may be ignored.[6]

Applicants respectfully submit the applied art does not meet this threshold burden. In particular, the outstanding Office Action asserts that Kim et al. and Magee discloses all the claimed limitations. Specifically, Applicants respectfully submit that neither Kim et al. nor Magee disclose the recited "CMOS semiconductor structure" of the claimed invention.

In addition, as stated above, "there must be no difference between the claimed invention and reference disclosure." Applicants respectfully submit that neither Kim et al. nor Magee disclose "an injection site associated with said CMOS semiconductor structure" that is compatible with modern CMOS technologies. Thus, there is a difference between the claimed invention and the reference disclosures of Kim et al. and Magee.

Kim et al. discloses an apparatus for decreasing latch-up in I/O circuits such as a data output buffer.[7] In particular, Kim et al. discloses an N-well guard ring **4** that is disposed under a data input and output pad **5**.[8] In addition, Kim et al. discloses the N-well guard ring **4** is not only formed on a portion adjacent to the P-well **2** and the N-well **3**, but also *formed on a portion of the P-type substrate under the data output pad* **5**, wherein the N-well guard ring **4** is formed as

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[1] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[2] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[3] *See* MPEP § 2131.
[4] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[5] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[6] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).
[7] Kim et al. ABSTRACT.
[8] *Id.* at FIG. 3, FIG. 4, column 2, lines 51-53.

a single enlarged N-well guard ring (emphasis added).[9]

Further, Kim et al. discloses that the N-well guard ring **4** does not have a separated structure such as the first and the second N-well guard rings **4A** and **4B** in CMOS technologies, but instead has a widely expanded and integrated structure.[10] Moreover, Kim et al. discloses that the minority carriers transmitted from the second N^+ region **23** to the first N^+ pickup region **34** of the PMOS transistor are completely captured by the expanded N-well guard ring **4**, thereby preventing generation of the latch-up in NMOS and PMOS technologies.[11]

However, Kim et al. nowhere discloses, as recited in independent claim 1:

> [a] *CMOS semiconductor structure* comprising: a substrate; a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; *an injection site associated with said CMOS semiconductor structure;* and a plurality of contact regions inter-spaced a varying distance between said circuit structures (emphasis added).

In addition, claim 22 recites similar language. That is, in contrast to Kim et al., the claimed invention is directed toward a modern CMOS semiconductor structure.

Further, though Kim et al. discloses an apparatus that decreases latch-up in NMOS and PMOS technologies, it is respectfully submitted that Kim et al. does *not* disclose:

(1) an apparatus with the "CMOS semiconductor structure" of the claimed invention; and

(2) an apparatus that is applicable to modern CMOS technologies.

[9] *Id.* at FIG. 3, FIG. 4, column 2, lines 53-56.
[10] *Id.* at FIG. 1, FIG. 2, column 2, lines 58-61.
[11] *Id.* at column 2, lines 61-65.

As discussed above, Kim et al. requires the use of the area under the I/O pad for expanding the N-well guard ring in order to prevent latch-up. In contrast to Kim et al., in the claimed invention and in more modern CMOS technologies *the area under I/O pads is not available because additional circuits are placed under the I/O pads* due to restraints on integrated circuit area and requirements for increased integrated circuit functionality. Due to these restraints and the density requirements of today's integrated circuits, the apparatus for latch-up prevention in Kim et al. is *not* applicable to modern CMOS technologies. Thus, Kim et al. does not disclose the "CMOS semiconductor structure" of the claimed invention and that is required in modern CMOS technologies.

Further, the structure/approach disclosed by Kim et al. of expanding the N-well guard ring to collect injected minority carriers to reduce latch-up is *not applicable* for non-standard latch-up tests "arising from a cable discharge event," as recited in claims 19 and 29. That is, the structure/approach of Kim et al. is not applicable for these latch-up tests because the "injection site associated with said CMOS semiconductor structure" during the recited "cable discharge event" would require an unreasonably large N-Well guard ring in the apparatus of Kim et al. in order to prevent latch-up.

Moreover, the expanded/large N-Well guard rings of Kim et al. would be very difficult to implement in a modern CMOS semiconductor structure because these large/expanded guard rings would increase the size of I/O cells of the integrated circuit and would result in a larger requirement for integrated circuit area for these cells and thus reduce integrated circuit density and functionality.

Therefore, at least for the reasons above, it is respectfully submitted that Kim et al. does not disclose, anticipate or inherently teach the claimed invention and that claims 1 and 22, and claims dependent thereon patentably distinguish thereover.

Claims 1, 7 and 11-14 were rejected under 35 U.S.C. 102(b) as being anticipated by Magee. Applicant respectfully traverses the rejection. The outstanding Office Action asserts that Magee discloses all the claimed limitations. Applicants respectfully disagree, as discussed below.

Magee discloses a bipolar lateral transistor that was compatible with "current NMOS or CMOS processing."[12] It should be noted that "current" at the time of the Magee patent disclosure was 1987. In particular, Magee discloses an npn lateral transistor structure that is formed in a very lightly doped p^- -type silicon substrate **11**.[13] In addition, Magee discloses a lightly doped n^- -type well **12** that is deeply diffused into the substrate **11** and a further lightly doped p^- -type well **13** that is diffused into the n^- -type well **12**.[14] Further, Magee discloses a p-type region **14** that is diffused to form the intrinsic base, together with a p^+ -type region to act as a base contact.[15] Furthermore, Magee discloses that N^+ regions are added for the emitter **16** and collector contact region **17**, during which the emitter is diffused through the same window as the base **14**, to end up with a narrow P region surrounding and self aligned to the emitter. Moreover, Magee discloses the contact region **17** provides a collector for lateral transistor action and a collector contact for vertical transistor action.[16]

However, Magee nowhere discloses, as recited in independent claim 1:

> [a] *CMOS semiconductor structure* comprising: a substrate; a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; *an injection site associated with said CMOS semiconductor structure;* and a plurality of contact regions inter-spaced a varying distance between said circuit structures (emphasis added).

[12] Magee at ABSTRACT and column 2, lines 29-35.
[13] Magee at column 1, lines 62-64.
[14] Magee at column 1, lines 64-66.
[15] Magee at column 1, lines 66-68.

That is, in contrast to the Magee patent issued in 1987, the claimed invention is directed toward modern "CMOS semiconductor structures," as recited in claim 1. As discussed above in regards to Kim et al., it is respectfully submitted that the apparatus and structure of Magee is not applicable to modern CMOS semiconductor structures that have restraints on integrated circuit area and requirements for increased integrated circuit density and functionality.

Further, Magee was directed toward building bipolar transistors in the current CMOS processes of 1987. However, Magee was not directed toward the problem of reducing latch-up in modern CMOS technologies or in the "CMOS semiconductor structure," as recited in claim 1.

Moreover, Magee discloses an arrangement of n+ and p+ taps that is not feasible in a modern "CMOS semiconductor structure" due to space constraints in modern CMOS technologies.[17] Thus, it is respectfully submitted that Magee teaches away from the claimed invention.

Therefore, at least for the reasons above, it is respectfully submitted that Magee does not disclose, anticipate or inherently teach the claimed invention and that claim 1, and claims dependent thereon patentably distinguish thereover.

[16] Magee at column 2, lines 5-7.
[17] *Id.* at FIG. 2.

Application No.: 10/605,699 Attorney Docket No.: 21806-00156-US

Conclusion

Based on the above amendments and arguments, Applicant respectfully submits that the application is in condition for allowance. If a fee is due, please charge Deposit Account No. 50-3223, under Order No. 21806-00156-US, from which the undersigned is authorized to draw.

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